



ELECTRONICS





TO

DATE: May. 15. 2008

SAMSUNG TFT-LCD

MODEL NO.: LTN154CT02-0

NOTE: Extension code [-0] → LTN154CT02-0 Surface type [Anti-Glare]

The information described in this SPEC is preliminary and can be changed without prior notice

APPROVED BY:

K. H. Shin

PREPARED BY: Application Engineering Part (Mobile)

SAMSUNG ELECTRONICS CO., LTD.



Samsung Secret

Doc.No. LTN154CT02-0 Rev.No

04-A00-S-080515

Page

1 / 31

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CONTENTS			Esperimenta kumpulum patropos, antopos, sata A
Revision History			(3)
General Descriptio	n		(4)
1. Absolute Maxim 1.1 Absolute Ra 1.2 Electrical Al	atings of environme		(5)
2. Optical Characte	eristics		(7)
3. Electrical Chara 3.1 TFT LCD Mo 3.2 Backlight Un	odule		(10)
4. Block Diagram 4.1 TFT LCD Mo 4.2 Backlight Un 4.3 Inverter Unit	it		(13)
9 9	& Power ace it ams of LVDS For		(14) h Color.
5.7 Inverter Sign6. Interface Timing6.1 Timing Para	meters ams of interface Si		(20)
7. Outline Dimension	on		(22)
8. Packing			(24)
9. Marking & Othe	rs		(25)
10. General Preca	ution		(27)
11. EDID Samsung Secret			(29)
122 124 124 124 124 124 124 124 124 124	O Barrier	04 400 0 000545	Pere 0 /04
Doc.No. LTN154CT02	-0 Rev.No	04-A00-S-080515	Page 2 / 31



REVISION HISTORY

Approval

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Date	Revision No.	Page	Summary						
Oct. 19. 2007	P00	All	LTN154CT02-0 model Preliminary spec was iss	ued first.					
Jan. 25. 2008	P01		Panel Rev. Code scheme was added						
Mar. 31. 2008	P02	7	Color coordinate of R, G, B were updated	or coordinate of R, G, B were updated					
May. 15. 2008	A00	All	Approval spec was issued						
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Ooc.No. LT	N154CT02-0	Rev	7.No 04-A00-S-080515	Page	3 /	3			

오기남03043581응용기술파트(Mobile)12925093 20080515195656 오병일5APL-5emi-DAM - DELLG

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GENERAL DESCRIPTION

DESCRIPTION

LTN154CT02-0 is a color active matrix TFT (Thin Film Transistor) liquid crystal display (LCD) that uses amorphous silicon TFT as switching devices. This model is composed of a TFT LCD panel, a driver circuit and a backlight unit. The resolution of a 15.4" contains 1920 x 1200 pixels and can display up to 262,144 colors. 6 O'clock direction is the optimum viewing angle.

FEATURES

- · High contrast ratio, high aperture structure
- 1920 x 1200 pixels resolution (16:10)
- High Color Gamut (Typical 72%)
- · Low power consumption
- Fast Response
- 2 CCFL(Y-stack)
- DE(Data enable) only mode
- 3.3V LVDS Interface
- Onboard EEDID chip
- RoHS Compliance
- Windows Vista Premium Logo compliance

APPLICATIONS

- Notebook PC
- If the usage of this product is not for PC application, but for others, please contact SEC

GENERAL INFORMATION

Item	Specification		Note
Display area	331.2(H) x 207.0(V) (15.4" diagonal)	mm	
Driver element	a-Si TFT active matrix		
Display colors	262,144		
Number of pixel	1920 x 1200 (WUXGA)	pixel	16 : 10
Pixel arrangement	RGB vertical stripe		
Pixel pitch	0.1725(H) x 0.1725(V)	mm	
Display Mode	Normally white		
Surface treatment	Haze 40, Hardness 3H		Anti-glare

Doc.No. LTN154CT02-0 Rev.No 04-A00-S-080515 Page 4 / 3	Doc.No.	LTN154CT02-0	Rev.No	04-A00-S-080515	Page	4 / 31
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Mechanical Information

		•				Predictive volume of the state of the state of the
Item		Min.	Тур.	Max.	Unit	Note
	Horizontal (H)	343.5	344.0	344.5	mm	
Module size	Vertical (V)	224.5	225.0	225.5	mm	
3120	Depth (D)	-	_	7.0	mm	(1)
	Weight	-	-	650	g	

Note (1) Measurement condition of outline dimension

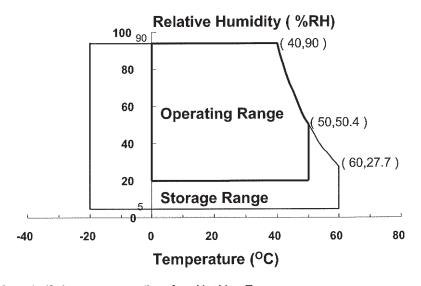
. Equipment : Vernier Calipers . Push Force : 500g ·f (minimum)

1. ABSOLUTE MAXIMUM RATINGS

1.1 ENVIRONMENTAL ABSOLUTE RATINGS

ltem	Symbol	Min.	Max.	Unit	Note
Storage temperate	TSTG	-20	60	°C	(1),(5)
Operating temperate (Temperature of glass surface)	TOPR	0	50	°C	(1),(5)
Shock (non-operating)	Snop	-	240	G	(2),(4)
Vibration (non-operating)	Vnop	-	2.41	G	(3),(4)

Note (1) Temperature and relative humidity range are shown in the figure below. 95 % RH Max. (40 °C \geq Ta) Maximum wet - bulb temperature at 39 °C or less. (Ta > 40 °C) No condensation



- (2) 2ms, half sine wave, one time for $\pm X$, $\pm Y$, $\pm Z$.
- (3) 5 500 Hz, random vibration, 30min for X, Y, Z.
- (4) At testing Vibration and Shock, the fixture in holding the Module to be tested have to be hard and rigid enough so that the Module would not be twisted or bent by the fixture.
- (5) If product is used for extended time excessively or exposed to high temperatures for extended time, there is a possibility of wide viewing angle film damage which could affect visual characteristics.

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Doc.No.	LTN154CT02-0	Rev.No	04-A00-S-080515	Page	5	/ 31



Approval

1.2 ELECTRICAL ABSOLUTE RATINGS

(1) TFT LCD MODULE

 V_{DD} =3.3V, V_{SS} = GND = 0V

ltem	Symbol	Min.	Max.	Unit	Note
Power Supply Voltage	V _{DD}	Vpp - 0.3	V _{DD} + 0.3	٧	(1)
Logic Input Voltage	Vin	VDD - 0.3	V _{DD} + 0.3	٧	(1)

Note (1) Within Ta (25 \pm 2 $^{\circ}\text{C}$)

(2) BACK-LIGHT UNIT

Ta = 25 ± 2 °C

Item	Symbol	Min.	Max.	Unit	Note
Lamp Current	lı.	2.0	7.0	mArms	(1)
Lamp frequency	FL	40	80	kHz	(1)

Note 1) Permanent damage to the device may occur if maximum values are exceeded Functional operation should be restricted to the conditions described under normal operating conditions.

Doc.No.	LTN154CT02-0	Rev.No	04-A00-S-080515	Page	6	/ 31	
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2. OPTICAL CHARACTERISTICS

The following items are measured under stable conditions. The optical characteristics should be measured in a dark room or equivalent state with the methods shown in Note (5). Measuring equipment: TOPCON BM-5A and PR-650

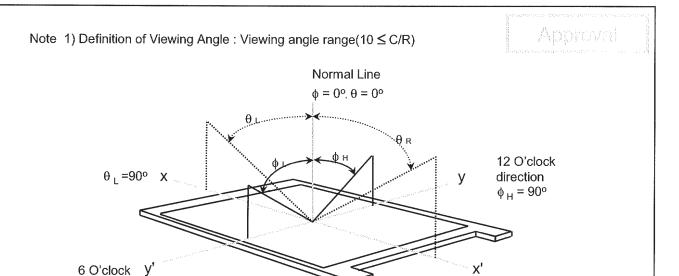
* Ta = 25 ± 2 °C, VDD=3.3V, fv= 60Hz, fDCLK = 82.1MHz, IL = 6.0 mA

	Γ	<u> </u>	1		I	z, IL = 6.0 MA		
ltem		Symbol	Condition	Min.	Тур.	Max	Unit	Note
	Contrast Ratio (5 Points)			400	500	_	_	(1), (2), (5)
Response Tir (Rising + F		TRT		-	16	20	msec	(1), (3)
Average Luminance of White (5 Points)		YL,AVE	Normal	290	340	_	cd/m ²	l∟=6.0mA (1), (4)
		Rx	Viewing	0.630	0.650	0.670		
	Red	Ry	Angle φ = 0	0.315	0.335	0.355		(1), (5) PR-650
	Green	Gx	$\theta = 0$	0.270	0.290	0.310	_	
Color	Green	Gy		0.585	0.605	0.625		
Chromaticity (CIE)	Blue	Bx		0.125	0.145	0.165		
	Dide	By	•	0.055	0.075	0.095		
	\\/hito	Wx		0.293	0.313	0.333		
	White	WY		0.309	0.329	0.349		
	11	θL		55	-	-		
Viewing	Hor.	θн	OD > 40	55	-	-	Dograda	(1), (5)
Angle	Ver.	фн	CR ≥ 10	45	-	-	Degrees	BM-5A
		фь		45	-	-		
Color Ga	mut			_	72	-	%	
13 Points White Variation		δι		-	-	1.7	-	(6)

Doc.No. LTN154CT02-0 Rev.No	04-A00-S-080515	Page	7 /3	1
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 $\theta_R = 90^{\circ}$

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Note 2) Definition of Contrast Ratio (CR): Ratio of gray max (Gmax), gray min (Gmin) at 5 points(4, 5, 7, 9, 10)

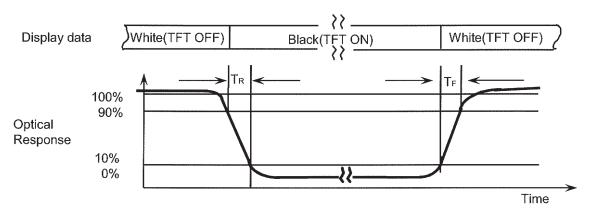
$$CR = \frac{CR(4) + CR(5) + CR(7) + CR(9) + CR(10)}{5}$$

 $\boxed{5}$, $\boxed{7}$, $\boxed{9}$, $\boxed{10}$ at the figure of Note (6). **Points**

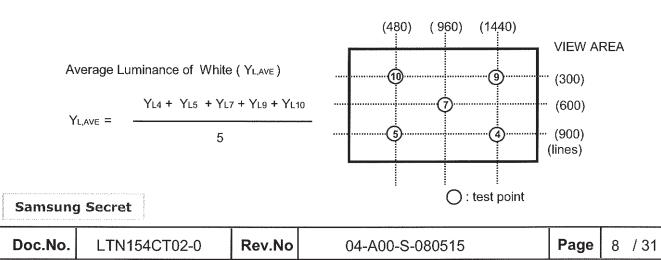
Note 3) Definition of Response time:

direction

 $\phi_L = 90^{\circ}$



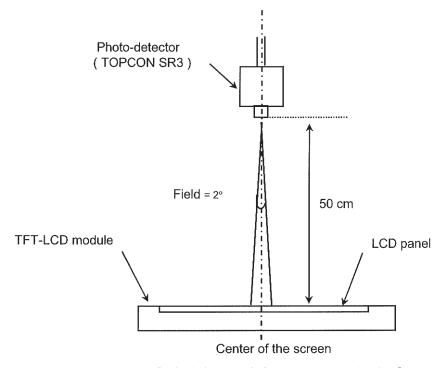
Note 4) Definition of Average Luminance of White: measure the luminance of white at 5 points.





Note 5) After stabilizing and leaving the panel alone at a given temperature for 30 min , the measurement should be executed. Measurement should be executed in a stable, windless, and dark room. 30 min after lighting the backlight. This should be measured in the center of screen. Lamp current: 6.0mA (Inverter: SIC-130T)

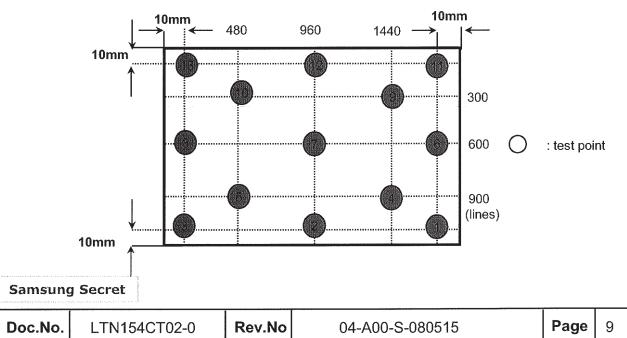
Environment condition: Ta = 25 ± 2 °C



[Optical characteristics measurement setup]

Note 6) Definition of 13 points white variation (δ L), CR variation (CVER) [(1) ~ (13)] Maximum luminance of 13 points

 $\delta L =$ Minimum luminance of 13 points



9 / 31



3. ELECTRICAL CHARACTERISTICS

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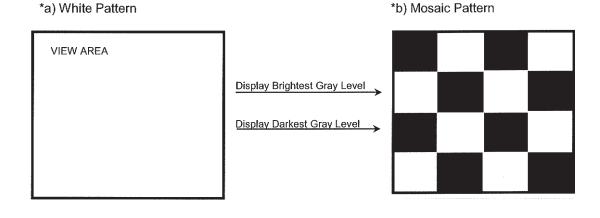
3.1 TFT LCD MODULE

Ta= 25 ± 2 °C

Item		Symbol	Min.	Тур.	Max.	Unit	Note
Voltage of Power	Supply	V _{DD}	3.0	3.3	3.6	٧	
Differential Input High		Vıн	-	-	+100	mV	V _{CM} = +1.2V
Voltage for LVDS Receiver Threshold	Low	VIL	-100	-	-	mV	
Vsync Frequency		fv	-	60	-	Hz	
Hsync Freque	ncy	fн	-	73	-	KHz	
Main Frequer	псу	fock	-	83.9	-	MHz	2CH
Rush Currer	nt	Irush	-	-	1.5	Α	(4)
	White		-	500	-	mA	(2),(3)*a
Current of Power Supply	Mosaic	loo	-	550	-	mA	(2),(3)*b
	V. stripe		-	720	820	mA	(2),(3)*c

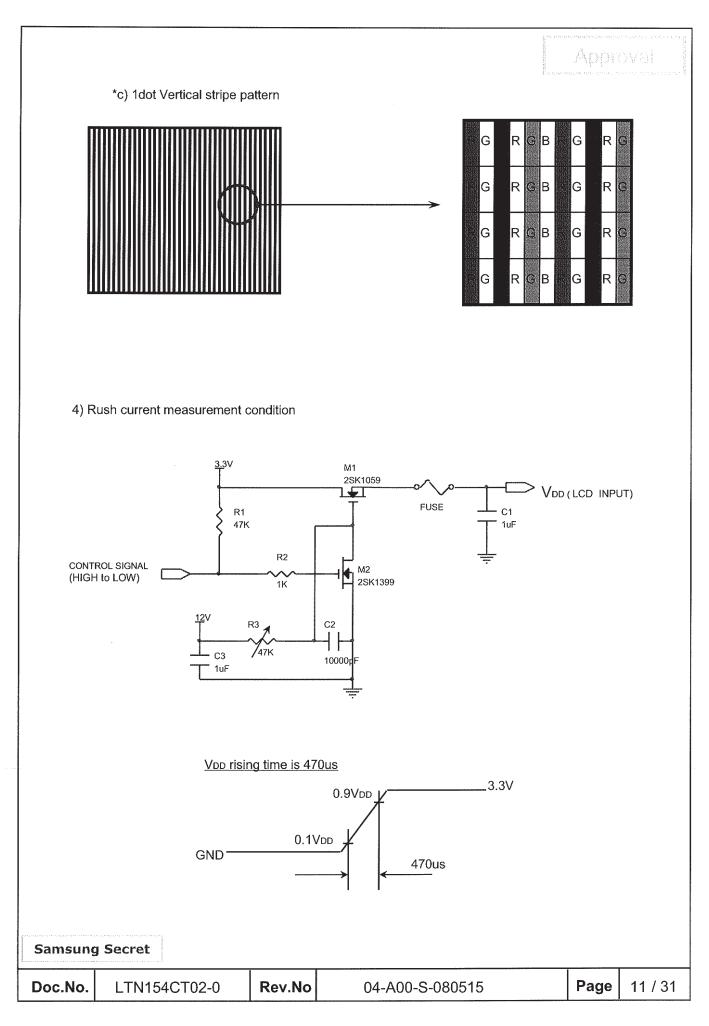
Note (1) Display data pins and timing signal pins should be connected.(GND = 0V)

- (2) $f_V = 60Hz$, $f_{DCLK} = 82.1MHZ$, $V_{DD} = 3.3V$, DC Current.
- (3) Power dissipation pattern



Doc.No.	LTN154CT02-0	Rev.No	04-A00-S-080515	Page	10 / 31	
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3.2 BACK-LIGHT UNIT

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The backlight system is an edge-lighting type with dual CCFL (Cold Cathode Fluorescent Lamp). The characteristics of a single lamp are shown in the following tables.

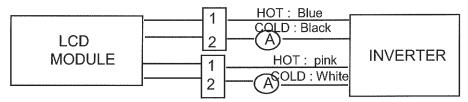
Ta= 25 ± 2 °C

Item	Symbol	Min.	Тур.	Max.	Unit	Note
Lamp Current	lı.	4.0	6.0	7.0	mArms	(1)
Lamp Voltage	VL	- 750		-	Vrms	I∟= 6.0mA
Frequency	fL	40	40 60 65 KHz		KHz	(2)
Power Consumption	PL	_	4.5		W	(3) IL = 6.0mA
Operating Life Time	Hr	15,000	-	_	Hour	(4)
Stortup Voltage	V/-			1180	Vrms	25°C, (5)
Startup Voltage	Vs	-	-	1415	Vrms	0°C, (5)

Note) The waveform of the inverter output voltage must be area symmetric and the design of the inverter must have specifications for the modularized lamp.

The performance of the backlight, for example life time or brightness, is much influenced by the characteristics of the DC-AC inverter for the lamp. So all the parameters of an inverter should be carefully designed so as not to produce too much leakage current from high-voltage output of the inverter. When you design or order the inverter, please make sure that a poor lighting caused by the mismatch of the backlight and the inverter(miss lighting, flicker, etc.) never occur. When you confirm it, the module should be operated in the same condition as it is installed in your instrument.

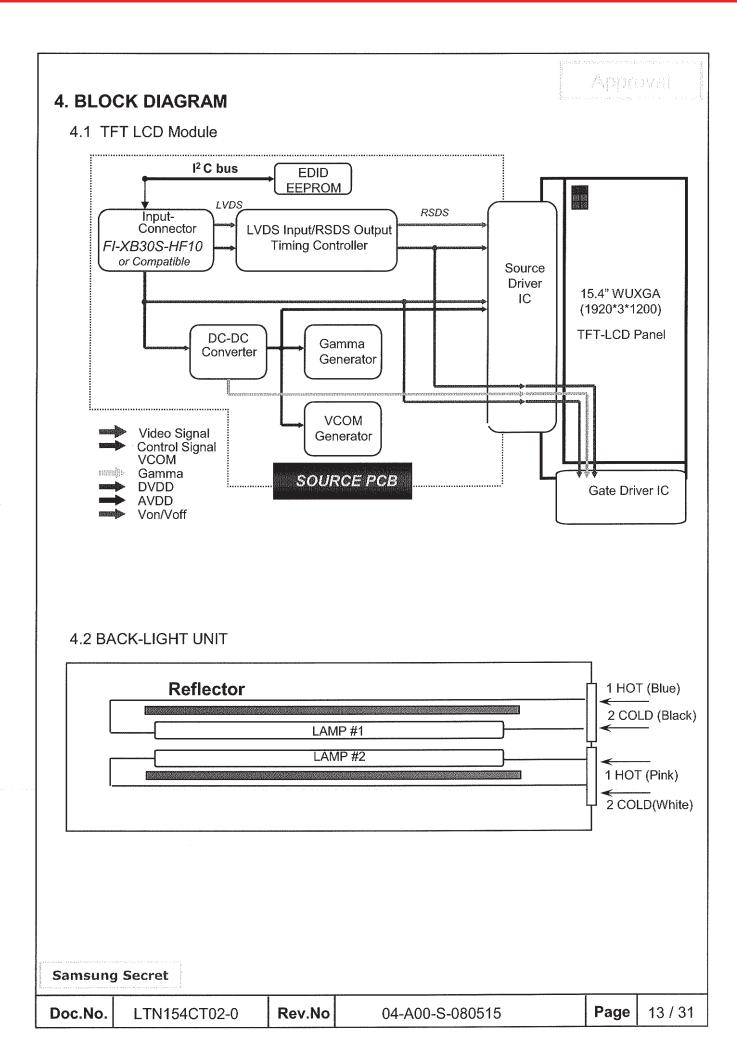
Note (1) Lamp current is measured with a high frequency current meter as shown below.



- (2) Lamp frequency may produce interference with horizontal synchronous frequency and this may cause line flow on the display. Therefore lamp frequency should be detached from the horizontal synchronous frequency and its harmonics as far as possible in order to avoid interference.
- (3) Refer to IL ×VL to calculate.
- (4) Life time (Hr) of a lamp can be defined as the time in which it continues to operate under the condition Ta= 25 ± 2 °C and IL = 6.0 mArms until one of the following event occurs.
 - 1. When the brightness becomes 50% or lower than the original.
 - 2. When the Effective ignition length becomes 80% or lower than the original value. (Effective ignition length is defined as an area that has less than 70% brightness compared to the brightness in the center point.)
- (5) The inverter open voltage this voltage should be measured after ballast capacitor- have to be larger than the lamp startup voltage, otherwise backlight may has blinking for a moment after turns on or not be turned on.
 - If an inverter has shutdown function it should keep its open voltage for longer than 1 second even if lamp connector open.

Doc.No. LTN154CT02-0 R	ev.No 04-A00-S-080515	Page	12 / 31	
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5. INPUT TERMINAL PIN ASSIGNMENT

5.1. Input Signal & Power (LVDS, Connector : JAE FI-XB30SRL-HF11 or compatible) Mating Connector : JAE FI-X30Sx or compatible)

No.	Symbol	Function	Polarity	Remarks
1	VSS	Ground		
2	VDD	POWER SUPPLY +3.3V		
3	VDD	POWER SUPPLY +3.3V		
4	VEEDID	DDC 3.3V Power		
5	NC	No Connection		
6	CLKEDID	DDC Clock		
7	DATAEDID	DDC data		
8	O_RxIN0-	LVDS Differential Data INPUT (Odd R0-R5,G0)	Negative	
9	O_RxIN0+	LVDS Differential Data INPUT (Odd R0-R5,G0)	Positive	
10	GND	Ground		
11	O_RxIN1-	LVDS Differential Data INPUT (Odd G1-G5,B0-B1)	Negative	
12	O_RxIN1+	LVDS Differential Data INPUT (Odd G1-G5,B0-B1)	Positive	
13	GND	Ground		
14	O_RxlN2-	LVDS Differential Data INPUT (Odd B2-B5,Sync,DE)	Negative	
15	O_RxIN2+	LVDS Differential Data INPUT (Odd B2-B5,Sync,DE)	Positive	
16	GND	Ground		
17	O_RxCLK-	LVDS Differential Data INPUT (Odd Clock)	Negative	
18	O_RxCLK+	LVDS Differential Data INPUT (Odd Clock)	Positive	
19	GND	Ground		
20	E_RxIN0-	LVDS Differential Data INPUT (Even R0-R5,G0	Negative	
21	E_RxIN0+	LVDS Differential Data INPUT (Even R0-R5,G0)	Positive	
22	GND	Ground		
23	E_RxIN1-	LVDS Differential Data INPUT (Even G1-G5,B0-B1)	Negative	
24	E_RxIN1+	LVDS Differential Data INPUT (Even G1-G5,B0-B1)	Positive	-
25	GND	Ground		
26	E_RxIN2-	LVDS Differential Data INPUT (Even B2-B5,Sync,DE)	Negative	
27	E_RxIN2+	LVDS Differential Data INPUT (Even B2-B5,Sync,DE)	Positive	
28	GND	Ground		
29	E_RxCLK-	LVDS Differential Data INPUT (Even Clock)	Negative	
30	E_RxCLK+	LVDS Differential Data INPUT (Even Clock)	Positive	

Doc.No.	LTN154CT02-0	Rev.No	04-A00-S-080515	Page	14 / 31
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Approval

5.2 LVDS Interface : Transmitter DS90CF363 or Compatible

LVDS for Odd pixel

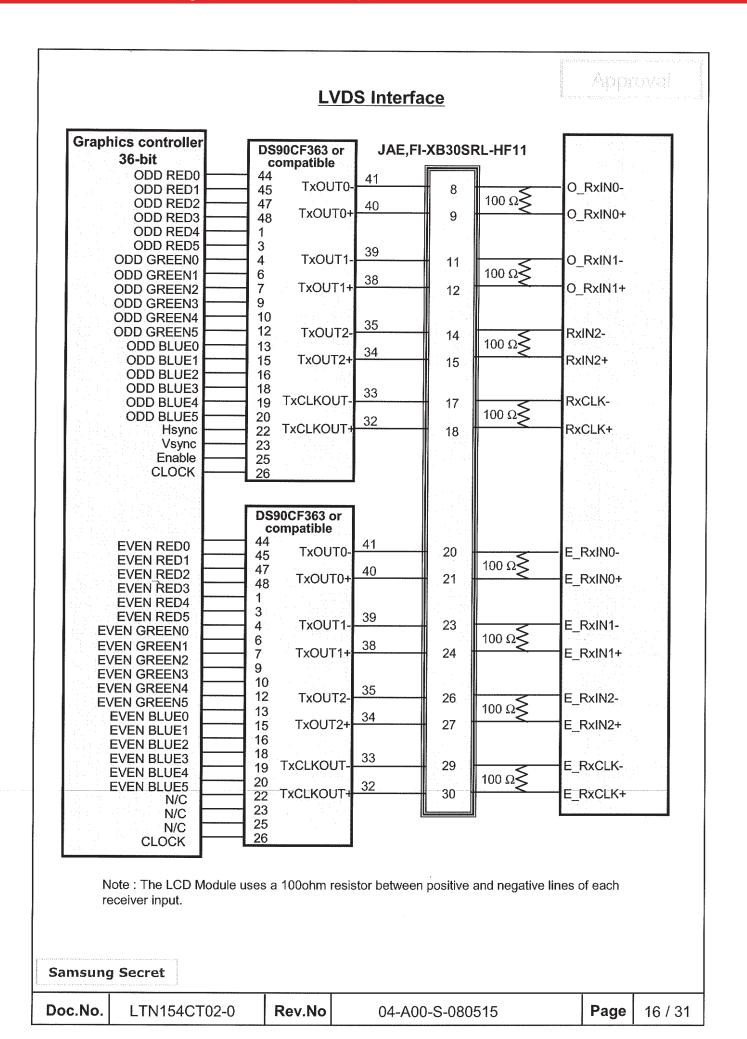
Pin No.	Name	RGB Signal	Pin No.	Name	RGB Signal	
44	TxIN0	RO0	12	TxIN11	GO5	
45	TxIN1	RO1	13	TxIN12	BO0	
47	TxIN2	RO2	15	TxIN13	BO1	
48	TxIN3	RO3	16	TxIN14	BO2	
1	TxIN4	RO4	18	TxIN15	BO3	
3	TxIN5	RO5	19	TxIN16	BO4	
4	TxIN6	GO0	20	TxIN17	BO5	
6	TxIN7	GO1	22	TxIN18	Hsync	
7	TxIN8	GO2	23	TxIN19	Vsync	
9	TxIN9	GO3	25	TxIN20	DE	
10	TxIN10	GO4	26	TxCLK IN	Clock	

LVDS for Even pixel

Pin No.	Name	RGB Signal	Pin No.	Name	RGB Signal
44	TxIN0	RE0	12	TxIN11	GE5
45	TxIN1	RE1	13	TxIN12	BE0
47	TxIN2	RE2	15	TxIN13	BE1
48	TxIN3	RE3	16	TxIN14	BE2
1	TxIN4	RE4	18	TxIN15	BE3
3	TxIN5	RE5	19	TxIN16	BE4
4	TxIN6	GE0	20	TxIN17	BE5
6	TxIN7	GE1	22	TxIN18	N/C
7	TxIN8	GE2	23	TxIN19	N/C
9	TxIN9	GE3	25	TxIN20	N/C
10	TxIN10	GE4	26	TxCLK IN	Clock

Doc.No.	LTN154CT02-0	Rev.No	04-A00-S-080515	Page	15 / 31	
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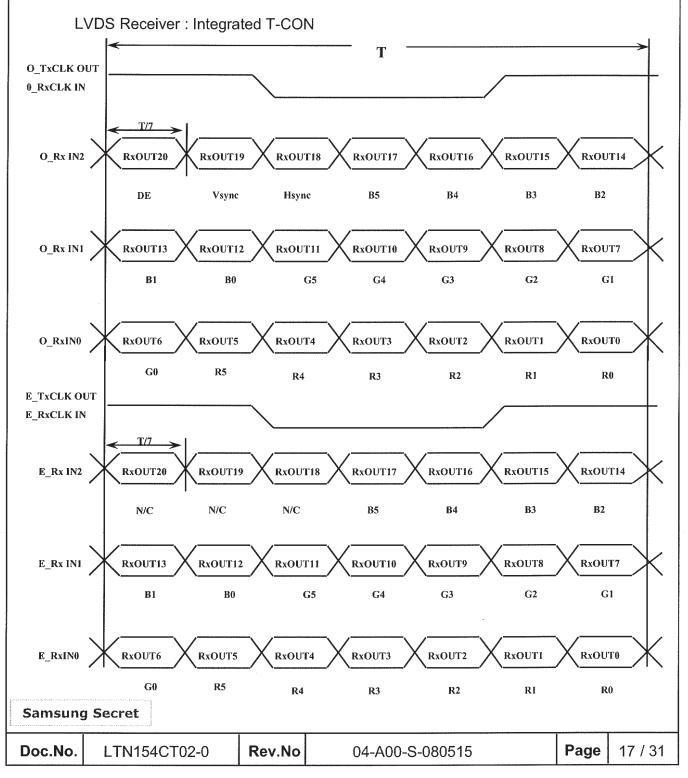
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Connector : JST BHSR - 02VS -1 Mating Connector : SM02B-BHSS-1(JST)

Pin NO.	Symbol Color		Function
1	НОТ	Pink / Blue	High Voltage
2	COLD	White / Black	Low Voltage

5.4 Timing Diagrams of LVDS For Transmission





5.5 Input Signals, Basic Display Colors and Gray Scale of Each Color

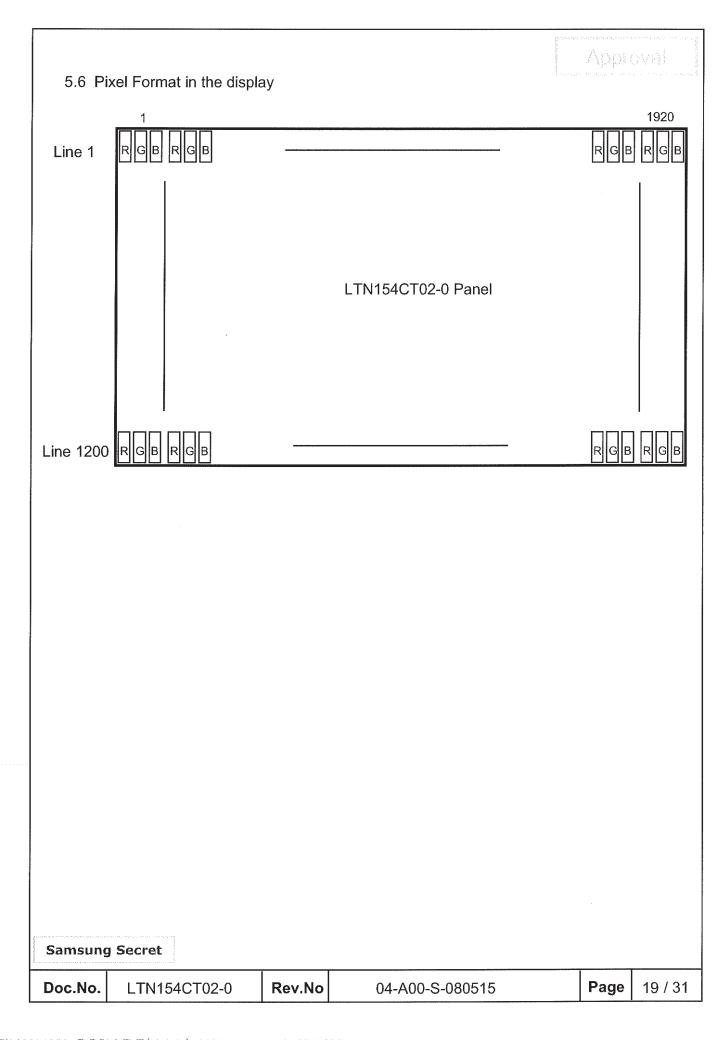
0.1	.							1]	Data		al								Gray
Color	Display				ed	I	l				en	Γ	Γ		Г		ue	Γ		Scale Level
		R0	R1	R2		R4	-		G1	G2	G3	G4	G5	B0	B1	B2	В3	45	B5	Level
	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	-
	Green	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0	-
Basic	Cyan	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	-
Colors	Red	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	-
	Magenta	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1	-
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	_
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	_
	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R0
	Dark	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R1
Gray	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R2
Scale	:	:	:	:	:	;	:	:	:	;	:	:	:	:	:	:	:	:	:	R3~R6
Of	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	110~111
Red	1	1	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	R61
	Light	0	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	R62
	Red	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	R63
	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	G0
	Dark	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	G1
Gray	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	G2
Scale	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:		:-	G3~G6
Of	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	G3~G
Green	\	0	0	0	0	0	0	1	0	1	1	1	1	0	0	0	0	0	0	G61
	Light	0	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	G62
	Green	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0	G63
	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	В0
	Dark	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	B1
Gray	1	0	0	0	0	0	-0	0	0	0	0	0	. 0	0	1	0	0	-0	0	B2
Scale	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	D0 D0
Of	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	B3~B60
Blue	\	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	1	B61
	Light	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	B62
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	B63

Note 1) Definition of gray:

Rn: Red gray, Gn: Green gray, Bn: Blue gray (n=gray level)

Note 2)Input signal: 0 =Low level voltage, 1=High level voltage

Doc.No.	LTN154CT02-0	Rev.No	04-A00-S-080515	Page	18 / 31	
						•





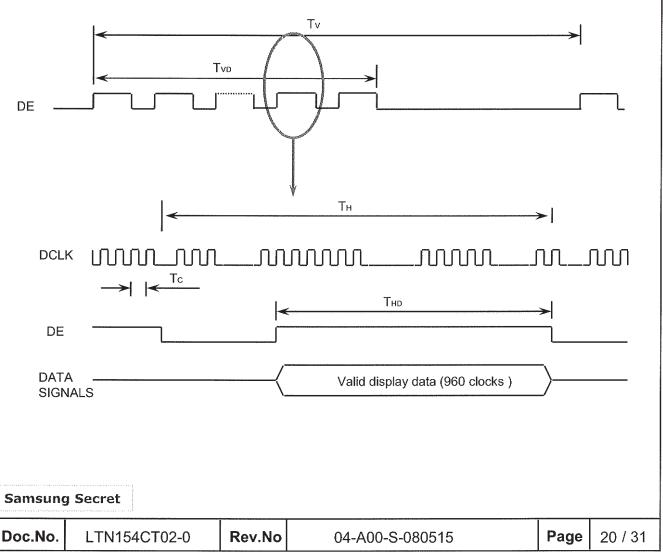
6. INTERFACE TIMING

Approval

6.1 Timing Parameters

Signal	Item	Symbol	Min.	Тур.	Max.	Unit	Note
Frame Frequency	Cycle	TV	1204	1250	1400	Lines	
Vertical Active Display Term	Display Period	TVD	-	1200	-	Lines	
One Line Scanning Time	Cycle	TH	1030	1080	1170	Clocks	
Horizontal Active Display Term	Display Period	THD	-	960	-	Clocks	

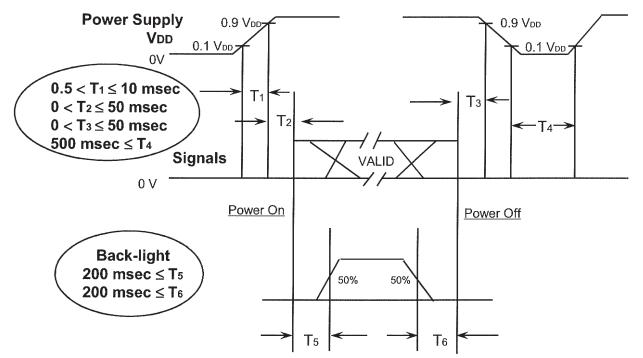
6.2 Timing diagrams of interface signal





6.3 Power ON/OFF Sequence

: To prevent a latch-up or DC operation of the LCD module, the power on/off sequence should be as the diagram below.



Power ON/OFF Sequence

T1: Vdd rising time from 10% to 90%

T2: The time from Vdd to valid data at power ON.

T3: The time from valid data off to Vdd off at power Off.

T4: Vdd off time for Windows restart

T5: The time from valid data to B/L enable at power ON.

T6: The time from valid data off to B/L disable at power Off.

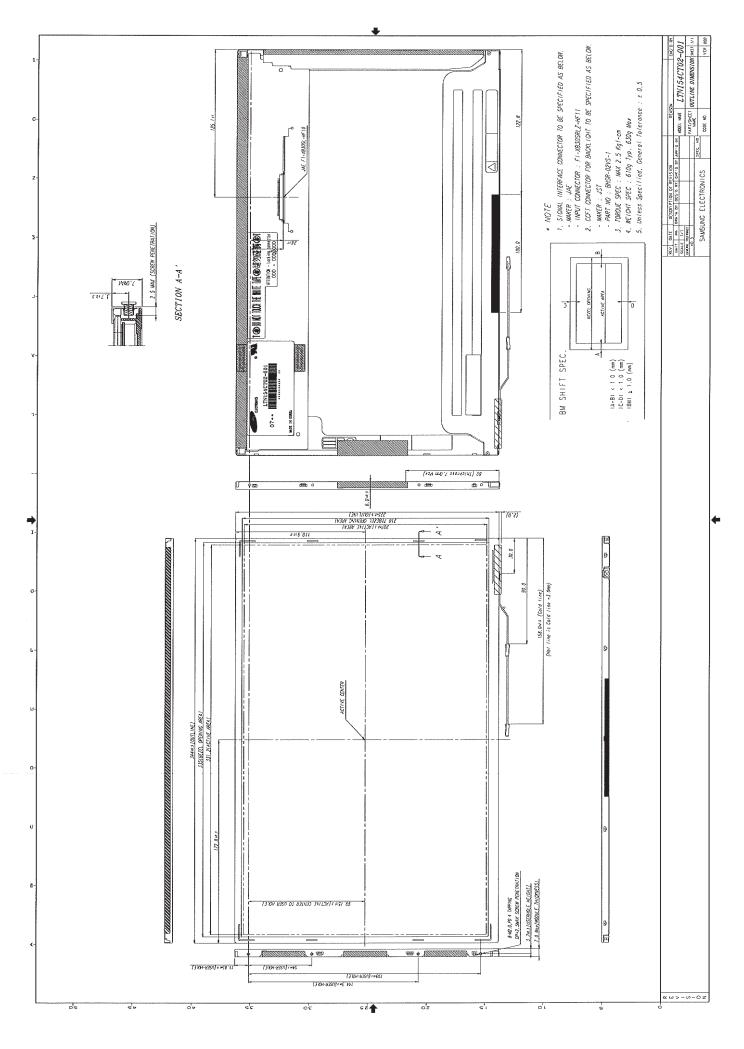
NOTE.

- (1) The supply voltage of the external system for the module input should be the same as the definition of VDD.
- (2) Apply the lamp voltage within the LCD operation range. When the back-light turns on before the LCD operation or the LCD turns off before the back-light turns off, the display may momentarily become white.
- (3) In case of VDD = off level, please keep the level of input signals on the low or keep a high impedance.
- (4) T4 should be measured after the module has been fully discharged between power off and on period.
- (5) Interface signal shall not be kept at high impedance when the power is on.

Sa	m	su	n	g S	ec	ret	t
----	---	----	---	-----	----	-----	---

Doc.No.	LTN154CT02-0	Rev.No	04-A00-S-080515	Page	21 / 31
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7. Mechanical Outline Dimension		Approval				
[Ref	er to the next page]			Eg. (1640) -	europea a Britistis un 140	
Samsung	Secret					
Doc.No.	LTN154CT02-0	Rev.No	04-A00-S-080515	5	Page	22 / 31
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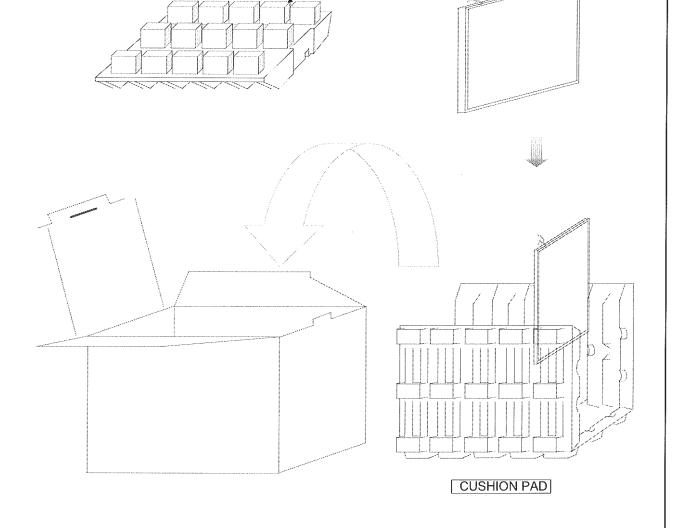
8. PACKING

- 1. CARTON(Internal Package)
 - (1) Packing Form
 Corrugated Cardboard box and Corrupad form as shock absorber

CUSHION CAP

PANEL

(2) Packing Method



Note 1)Total Weight : Approximately 10 kg

2) Acceptance number of piling: 10 sets 3) Carton size: 376(W) X 326(D) X 404(H)

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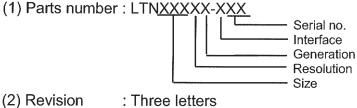
 Doc.No.
 LTN154CT02-0
 Rev.No
 04-A00-S-080515
 Page
 24 / 31

(3)Packing Material

No	Part name	Quantity
1	Static electric protective sack	10 pcs
2	Packing case (Inner box) included shock absorber	1 set
3	Pictorial marking	2 pcs
4	Carton	1 set

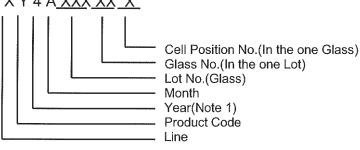
9. MARKINGS & OTHERS

A nameplate bearing followed by is affixed to a shipped product at the specified location on each product.



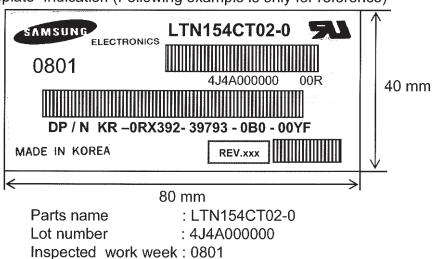
: X Y 4 A XXX XX X

(3) Lot number



NOTE 1). This code indicating year is omitted in the products of KIHENG site.

(4) Nameplate Indication (Following example is only for reference)

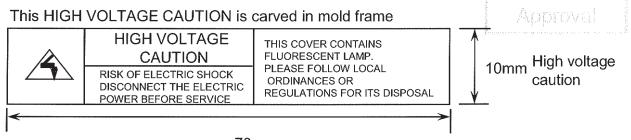


: Dell Part Number ("0RX392" is for 154CT02-0) DP/N

Samsung Secret REV.xxx : Product Revision Code (Refer to the next page)

Doc.No. LTN154CT02-0 Rev.No 04-A00-S-080515 Page 25 / 31 Global LCD Panel Exchange Center



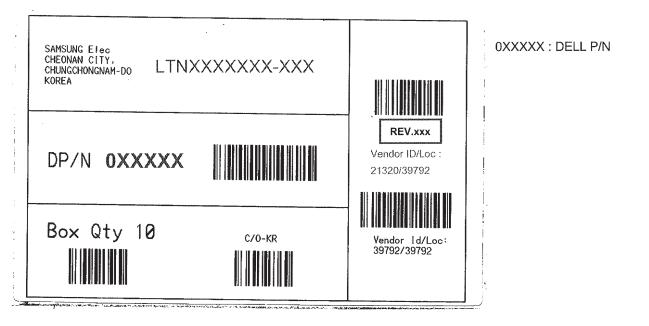


70_{mm}

* Panel revision code scheme (Refer to the Red box on the label)

Build Name(s)	Revision Code(s)
SST (WS)	X00, X01, X02, X09
PT (ES)	X10, X11, X12, X19
ST (CS)	X20, X21, X23, X29
XB (MP)	A00, A01, A02, A99

(6) Packing small box attach (Following example is only for reference)



(7) Packing box Marking: Samsung TFT-LCD Brand Name



Doc.No.	LTN154CT02-0	Rev.No	04-A00-S-080515	Page	26 / 31



10. GENERAL PRECAUTIONS

Approval

1. Handling

- (a) When the module is assembled, It should be attached to the system firmly using every mounting holes. Be careful not to twist and bend the modules.
- (b) Refrain from strong mechanical shock and / or any force to the module. In addition to damage, this may cause improper operation or damage to the module and CCFT backlight.
- (c) Note that polarizers are very fragile and could be easily damaged. Do not press or scratch the surface harder than a HB pencil lead.
- (d) Wipe off water droplets or oil immediately. If you leave the droplets for a long time, Staining and discoloration may occur.
- (e) If the surface of the polarizer is dirty, clean it using some absorbent cotton or soft cloth.
- (f) The desirable cleaners are water, IPA(Isoprophyl Alcohol) or Hexane.

 Do not use Ketone type materials(ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanent damage to the polarizer due to chemical reaction.
- (g) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, legs or clothes, it must be washed away thoroughly with soap.
- (h) Protect the module from static, it may cause damage to the C-MOS Gate Array IC.
- (i) Use fingerstalls with soft gloves in order to keep display clean during the incoming inspection and assembly process.
- (j) Do not disassemble the module.
- (k) Do not pull or fold the lamp wire.
- (I) Do not adjust the variable resistor which is located on the back side.
- (m) Protection film for polarizer on the module shall be slowly peeled off just before use so that the electrostatic charge can be minimized.
- (n) Pins of I/F connector shall not be touched directly with bare hands.

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Doc.No.	LTN154CT02-0	Rev.No	04-A00-S-080515	Page	27 / 31
DOC.NO.	L1N134C102-0	Rev.NO	04-A00-3-060313		21/31



2. STORAGE

- Approval
- (a) Do not leave the module in high temperature, and high humidity for a long time. It is highly recommended to store the module with temperature from 0 to 35 °C and relative humidity of less than 70%.
- (b) Do not store the TFT-LCD module in direct sunlight.
- (c) The module shall be stored in a dark place. It is prohibited to apply sunlight or fluorescent light during the store.

3. OPERATION

- (a) Do not connect, disconnect the module in the "Power On" condition.
- (b) Power supply should always be turned on/off by following item 6.3 "Power on/off sequence ".
- (c) Module has high frequency circuits. Sufficient suppression to the electromagnetic interference shall be done by system manufacturers. Grounding and shielding methods may be important to minimize the interference.
- (d) The cable between the backlight connector and its inverter power supply shall be a minimized length and be connected directly. The longer cable between the backlight and the inverter may cause lower luminance of lamp(CCFT) and may require higher startup voltage(Vs).
- (e) The standard limited warranty is only applicable when the module is used for general notebook applications. If used for purposes other than as specified, SEC is not to be held reliable for the defective operations. It is strongly recommended to contact SEC to find out fitness for a particular purpose.

4. OTHERS

- (a) Ultra-violet ray filter is necessary for outdoor operation.
- (b) Avoid condensation of water. It may result in improper operation or disconnection of electrode.
- (c) Do not exceed the absolute maximum rating value. (the supply voltage variation, input voltage variation, variation in part contents and environmental temperature, so on)

 Otherwise the module may be damaged.
- (d) If the module displays the same pattern continuously for a long period of time, it can be the situation when the image "sticks" to the screen.
- (e) This module has its circuitry PCB's on the rear side and should be handled carefully in order not to be stressed.

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Doc.No.	LTN154CT02-0	Rev.No	04-A00-S-080515	Page	28 / 31	
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	Byte	Field Name and Comments	Value	Value
	(hex)	n ne engant ne ety talada anyila	(hex)	(binary)
	0	Header	00	00000000
-	1	Header	FF F	11111111
Header	2	Header	FF	11111111
8	3	Header	FF F	11111111
₽	4	Header	FF	11111111
_	5	Header	FF	111111111
	6	Header	FF	11111111
	7	Header	00	00000000
-	8	EISA manufacture code = 3 Character ID	4C	01001100
	9	EISA manufacture code (Compressed ASCII)	A3	10100011
;	0A	Panel Supplier Reserved – Product Code	43	01000011
ersion	OB	Panel Supplier Reserved – Product Code	54	01010100
Version	OC.	LCD module Serial No - Preferred but Optional ("0" if not used)	00	00000000
Ф >	OD	LCD module Serial No - Preferred but Optional ("0" if not used)	00	00000000
	0E	LCD module Serial No - Preferred but Optional ("0" if not used)	00	00000000
	OF	LCD module Serial No - Preferred but Optional ("0" if not used)	00	00000000
> Old	10	Week of manufacture	00	00000000
	11	Year of manufacture	12	00010010
	12	EDID structure version # = 1	01	00000001
	13	EDID revision # = 3	03	00000011
2	14	Video I/P definition = Digital I/P	90	10010000
Parameters	15	Max H image size = (Rounded to cm)	21	00100001
5 E	16	Max V image size = (Rounded to cm)	15	00010101
) <u>@</u> [17	Display gamma = (gamma ×100)-100 = Example: (2.2 × 100) - 100 = 120	78	01111000
α Γ	18	Feature support (no DPMS, Active off, RGB, timing BLK 1)	OA	00001010
	19	Red/Green Low bit (RxRy/GxGy)	87	10000111
-	1A	Blue/White Low bit (BxBy/WxWy)	F5	11110101
· m	1B	Red X Rx = 0.xxx	94	10010100
) <u>H</u>	1C	Red Y Ry = 0.xxx	57	01010111
<u> </u>	1D	Green X Gx = 0.xxx	4F	01001111
Coordinates	1E	Green Y Gy = 0.xxx	8C	10001100
8	1F	Blue X Bx = 0.xxx	27	00100111
· () =	20	Blue Y By = 0.xxx	27	00100111
	21	White X Wx = 0.xxx	50	01010000
	22	White Y Wy = 0.xxx	54	01010100
Estabilished	23	Established timings 1 (00h if not used)	00	00000000
	23 24	Established timings 2 (00h if not used)	00	00000000
	25	Manufacturer's timings (00h if not used)	00	00000000

Doc.No.	LTN154CT02-0	Rev.No	04-A00-S-080515	Page	29 / 31

26 Standard timing (TD) (01) if not known)				5-2-10-1-2-1-2-1	otsky someovonovko iskninka uskisokni u isno nikinsunkink
27 Shandard tening IDZ (Dit in cot uses)					
2 Standard Image [D2] (D1) if not used)		26	Standard timing ID1 (01h if not used)	01	00000001
2 Standard timing IDS (Dith Find tuesch)		27	Standard timing ID1 (01h if not used)	01	00000001
2 Standard timing ID2 (01 hif not users)		28		01	00000001
20				Π1	
32 Standard tuning IDT (Olth if not used)	Ωg				
32 Standard tuning IDT (Olth if not used)					
32 Standard tuning IDT (Olth if not used)	. <u>≒</u>	***************************************			
32 Standard tuning IDT (Olth if not used)	_ <u>;</u> ⊑				
32 Standard tuning IDT (Olth if not used)					
32 Standard tuning IDT (Olth if not used)	<u>S</u>				
32 Standard tuning IDT (Olth if not used)	ρ				
32 Standard tuning IDT (Olth if not used)	ğ				
33 Standard timing IDF, (Oth Ari not used)	(A)			*****	
34 Standard timing IDS (Oth if not use d)			Standard timing ID7 (01h if not used)		
35 Standard timing LIX (Olth if not used)		33	Standard timing ID7 (01h if not used)	01	00000001
36		34	Standard timing ID8 (01h if not used)	01	00000001
37 Pixel Clock/10,000		35	Standard timing ID8 (01h if not used)	01	00000001
37 Fixed Clock/10,000 (MSE) 40 010000000		36	Pixel Clock/10,000 (LSB)	24	00100100
38		37		40	01000000
39					
3A Horizontal Active Act					
38			<u> </u>		
32 Vertical Ellanking (T-Vp) xxxx lines (DE Ellanking typ, for DE only penels) 23 00100011			<u> </u>		
3D					
3E					
1906 1907 1908		ļ			
Bit[7] 0: Non-interlace, 1: Interlace	7				
Bit[7] 0 : Non-interlace, 1: Interlace	<u>⊬</u> -₩				
Bit[7] 0 : Non-interlace, 1: Interlace	je	40			
Bit[7] 0 : Non-interlace, 1: Interlace	ii.	41	Horizontal Vertical Sync Offset/Width upper 2 bits		
Bit[7] 0 : Non-interlace, 1: Interlace	SS	42	Horizontal Image Size =xxx mm	4B	01001011
Bit[7] 0 : Non-interlace, 1: Interlace	9	43	Vertical image Size = xxx mm	CF	11001111
Bit[7] 0 : Non-interlace, 1: Interlace]6	44	Horizontal Image Size / Vertical image size	10	00010000
Bit(7] 0 Non-interface, 1: Interface	.⊑	45		00	00000000
Bit(7] 0 Non-interface, 1: Interface	.E.				
Bit[6-5] 00. Mornal display, no etero, XX. See table xx for definition	-				000000
Referenced Default = 1Ah		47	Bit[2:1] :The interpretation of bits 2 and 1 is dependent on the decode of bits 4 and 3 - see Table 3.18.	1A	
49 Fixel Clock/10,000					
Horizontal Active = xxxx pixels (lower 8 bits) 80 10000000					
AB		49			
C		4A	Horizontal Active = xxxx pixels (lower 8 bits)	80	10000000
4D Vertical Active = xxxx lines B0 10110000		4B	Horizontal Blanking (Thbp) = xxxx pixels (lower 8 bits)	28	00101000
4D Vertical Active = xxxx lines B0 10110000		4C	Horizontal Active/Horizontal blanking (Thbp) (upper4:4 bits)	71	01110001
Vertical Blanking (Tvbp) = xxxx lines (DE Blanking typ. for DE only panels) 23 00100011		4D		B0	10110000
4F Vertical Active : Vertical Blanking (Tvbp) (upper4:4 bits) 40 01000000					
So					
Signature Sign					
Bit[7] 0: Non-interlace, 1: Interlace Bit[6:5] 00: Normal display, no strero, XX: See table xx for definition Bit[4:3] 00: Analog composite, 01: Bipolar analog composite, 10: Digital composite, 11: Digital separate 59 Bit[2:1] :The interpretation of bits 2 and 1 is dependent on the decode of bits 4 and 3 - see Table 3.18. Bit[0] :See Table VESA EDID spec for definition Referenced Default = 1Ah 00011010	¥				
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Bit[7] 0: Non-interlace, 1: Interlace Bit[6:5] 00: Normal display, no strero, XX: See table xx for definition Bit[4:3] 00: Analog composite, 01: Bipolar analog composite, 10: Digital composite, 11: Digital separate 59 Bit[2:1] :The interpretation of bits 2 and 1 is dependent on the decode of bits 4 and 3 - see Table 3.18. Bit[0] :See Table VESA EDID spec for definition Referenced Default = 1Ah 00011010	Ŏ				
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Bit[7] 0: Non-interlace, 1: Interlace Bit[6:5] 00: Normal display, no strero, XX: See table xx for definition Bit[4:3] 00: Analog composite, 01: Bipolar analog composite, 10: Digital composite, 11: Digital separate 59 Bit[2:1] :The interpretation of bits 2 and 1 is dependent on the decode of bits 4 and 3 - see Table 3.18. Bit[0] :See Table VESA EDID spec for definition Referenced Default = 1Ah 00011010	Ė	57	Horizontal Border = 0 (Zero for Notebook LCD)		
Bit[7] 0: Non-interlace, 1: Interlace Bit[6:5] 00: Normal display, no strero, XX: See table xx for definition Bit[4:3] 00: Analog composite, 01: Bipolar analog composite, 10: Digital composite, 11: Digital separate 59 Bit[2:1] :The interpretation of bits 2 and 1 is dependent on the decode of bits 4 and 3 - see Table 3.18. Bit[0] :See Table VESA EDID spec for definition Referenced Default = 1Ah 00011010	i≡	58	Vertical Border = 0 (Zero for Notebook LCD)	00	00000000
Bit[6:5] 00: Normal display, no strero, XX: See table xx for definition Bit[4:3] 00: Analog composite, 01: Bipolar analog composite, 10: Digital composite, 11: Digital separate 59 Bit[2:1] :The interpretation of bits 2 and 1 is dependent on the decode of bits 4 and 3 - see Table 3.18. Bit[0] :See Table VESA EDID spec for definition Referenced Default = 1Ah 00011010		j.			
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59 Bit[2:1] :The interpretation of bits 2 and 1 is dependent on the decode of bits 4 and 3 - see Table 3.18. Bit[0] :See Table VESA EDID spec for definition Referenced Default = 1Ah 5amsung Secret		[·			
Referenced Default = 1Ah 00011010 Samsung Secret		. 59	Bit[2:1] :The interpretation of bits 2 and 1 is dependent on the decode of	1A	
Samsung Secret			Bit[0] :See Table VESA EDID spec for definition		00044515
No. No. TN4540T02.0	Samsu	ng Sec		<u> </u>	1 00011010
JOC.NO. LIN 546 UZ-U REV.NO U4-AUU-5-U6U5 Faue 50 /	oc.No). L	TN154CT02-0 Rev.No 04-A00-S-080515	·	Page 30 / 3

				Aggr	aval.
	5A	Flag	00	000	00000
	5B	Flag	00	000	00000
	5C	Fiag	00		00000
	5D	Data Type Tag: Alphanumeric Data String (ASCII)	FE		11110
	5E	Flag	00		00000
	5F	Deli P/N 1 st Character	52		10010
	60	Dell P/N 2 nd Character	58		11000
	61	Dell P/N 3 rd Character	33		10011
က္က	62	Dell P/N 4 th Character	39		11001
単語	63	Dell P/N 5 th Character	32		10010
Timing Descripter #3 Dell specific information	64	LCD Supplier EEDID Revision # Bit[7]: 0=X, 1=A Bit[6:0]: 00, 01, 02 for SST 10, 11, 12 for PT 20, 21, 22 for ST 00, 01, 02 for X-Build (if Bit[7]=1)	80		
					00000
	65	Manufacturer P/N	31		10001
	66	Manufacturer P/N	35		10101
	67	Manufacturer P/N	34	001	10100
	68	Manufacturer P/N	43	010	00011
	69	Manufacturer P/N	54	010	10100
	6A	Manufacturer P/N	0A	000	01010
	6 B	Manufacturer P/N (If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	20	001	00000
	6C	Flag	00	000	00000
	6D	Flag	00	000	00000
	6E	Flag	00	000	00000
	6F	Data Type Tag: Manufacturer Specified Data 00	FE	111	11110
	70	Flag	00	000	00000
	71	SMBUS Value = XX nits	00	000	00000
	72	SMBUS Value = XX nits	00	000	00000
	73	SMBUS Value = XX nits	00	000	00000
Ŧ	74	SMBUS Value = XX nits	00	000	00000
<u></u>	75	SMBUS Value = XX nits	00	000	00000
i <u>d</u>	76	SMBUS Value = XXX nits	00	000	00000
၁၄	77	SMBUS Value = XXX nits	00	000	00000
ă	78	SMBUS Value = max nits (Typically = 00h, XXX nits)	00	000	00000
Timing Descripter #4	79	Bit[7:3] Reserved Bit[2] 0: No RTC support, 1: RTC support Bit[1:0] 00: reserved, 01: single LVDS, 10: dual LVDS, 11: reserved 01h single channel LVDS, no RTC support 02h dual channel LVDS, no RTC support 05h single channel LVDS, with RTC support 06h dual channel LVDS, with RTC support	02		00010
	7A	BIST Enable: Yes = '01' No = '00'	01	000	00001
	7B	(If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	0A	00001010	
	7C	(If < 13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	20 20		00000
Checksum	7D	(If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)		001	00000
	7E	Extension flag (# of optional 128 EDID extension blocks to follow, Typ = 0)	00	00000000	
ا ا			ED		
	ng Sec	Checksum (The 1-byte sum of all 128 bytes in this EDID block shall = 0)		111	01101
oc.No). L1	TN154CT02-0 Rev.No 04-A00-S-080515		Page	31 / 3